TED (15) – 3131 Reg. No.....

(REVISION — 2015) Signature .....

DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/ MANAGEMENT/COMMERCIAL PRACTICE — APRIL, 2019

COMPUTER ARCHITECTURE

[*Time* : 3 hours

(Maximum marks : 100)

PART — A

(Maximum marks : 10)

Marks

I Answer *all* questions in one or two sentences. Each question carries 2 marks.

1. List the components of a computer.
2. Define rotation delay.
3. Write the need of User-visible register.
4. List the two basic tasks performed by micro programmed control unit.
5. Define fetch overlap. (5×2 = 10)

PART — B

(Maximum marks : 30)

II Answer any *five* of the following questions. Each question carries 6 marks.

1. Describe the memory hierarchy with a diagram.
2. Explain the Von-Neumann machine.
3. Describe magnetic disk read and write mechanism.
4. Explain programmed driven I/O.
5. Write short note on control and status registers.
6. Explain indirect cycle.
7. Explain advantages and disadvantages of microprogramming. (5×6 = 30)

Marks

PART — C

(Maximum marks : 60)

(Answer *one* full question from each unit. Each full question carries 15 marks.)

UNIT — I

III (a) Explain the elements of bus design. 8

(b) Describe the characteristics of memory system. 7

OR

IV (a) Explain interrupt and instruction cycle with diagram. 8

(b) Explain types of ROM. 7

UNIT — II

V (a) Explain disk performance parameters. 8

(b) Describe the Direct Memory Access (DMA). 7

OR

VI (a) List and compare different RAID levels. 8

(b) Explain interrupt driven I/O. 7

UNIT — III

VII (a) Describe the operations that must be performed by the processor. 8

(b) Explain instruction pipelining. 7

OR

VIII (a) Explain internal structure of the CPU with diagram. 8

(b) Explain advantages and disadvantages of condition codes. 7

UNIT — IV

IX (a) Explain the functioning of the micro programmed control unit with diagram. 8

(b) Explain micro operations involved in a fetch cycle. 7

OR

X Draw and explain different types of parallel organization. 15