DE & MP. 1

TED(15) -- 4032

(REVISION—2015)

Reg. No .....

Signature.....

MODEL QUESTION PAPER

FOURTH SEMESTER DIPLOMA EXAMINATION IN ELECTRICAL AND ELECTRONICS ENGINEERING -- APRIL 2017

DIGITAL ELECTRONICS AND MICROPROCESSOR

(Maximum Marks : 100) [Time : 3 hours

PART—A

(Maximum Marks : 10)

I Answer the following questions in one or two sentences. Each question carries 2 Marks.

1. Define the term 'Byte' in binary number system with an example.
2. Name any two basics gates and draw their symbols
3. Draw the symbols of positive and negative edge triggered RS Flip Flop
4. List different types of shift registers based on data storage and read
5. Define the term Microprocessor

(5x2=10)

PART-- B

II Answer any *five* of the following questions. Each question carries 6 Marks

1. Convert the binary number **(1001011.01101)** $_2$ to decimal. Show the steps.
2. Construct a Gate circuit with output expression $Y = \overline{AB + CD + EF}$ using basic gates
3. State and explain De Morgan's theorems.
4. Draw the schematic diagram of a 4 x1 Multiplexer and write its truth table
5. Draw the schematic diagram of a 3 bit Parrallel In Parallel Out shift register using negative edge triggered D Flip Flop and explain how a data 110 is stored .
6. Explain the concept of R-2R ladder network for Digital to Analogue Conversion.
7. List any six features of 8085 Microprocessor.

(5x6= 30)

PART C

(Answer one *full* question from each unit. Each question carries 15 Marks.)

MODULE 1

III

(a) Execute the following operation after converting the decimal numbers to equivalent binary number and convert the result back to decimal number

$(378.625)_{10} + (56.375)_{10}$ (10)

(b) Explain the operation of NAND and NOR Gates with Truth Table (5)

OR

IV

(a) Compare TTL, ECL and CMOS Logic Families (10)

(b) Convert the following decimal numbers to equivalent hex numbers. Show the steps

$(10767.93875)_{10}$ (5)

MODULE II

V

a) Construct a Half adder circuit using NAND Gates and explain its operation. (10)

b) Draw the Schematic diagram of a 1 x 4 De Multiplexer and write its Truth Table (5)

OR

VI

a. Explain the working of a 2 to 4 decoder (10)

b. Apply De Morgan's Theorems to the following expression and simplify it:

$\overline{(A\overline{B} + \overline{C}D + EF)}$ (5)

MODULE III

VII

a) Implement a **MOD 16** Synchronous binary UP counter with a negative edge-triggered *J-K* flip-flops and write count sequence with the waveforms (15)

OR

VIII

a) Explain how a data **1100** is stored in a register using a Serial In Parallel Out Right Shift Register (use Negative edge Triggered JK Flip Flop) (10)

b) Explain the working of Ramp Type Analogue to Digital convertor (5)

MODULE IV

IX

a) Draw and explain the internal architecture of 8085 Microprocessor (15)

OR

X

a) Explain with examples various groups of instructions in 8085 Microprocessor. (10)

b) Explain the addressing modes of 8085 Microprocessor (5)